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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/089,588 | 07/15/2002 | Daniel Bois | 5310-04500 | 2551 |

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| EXAMINER | |
|---|---|
| PHAM, LONG | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2814 | |

DATE MAILED: 09/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) |
|---|---|---|
| | 10/089,588 | BOIS ET AL. |
| | Examiner | Art Unit |
| | Long Pham | 2814 |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-15 and 20-28* is/are pending in the application.

4a) Of the above claim(s) *21-28* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15 and 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *04/21/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Election/Restrictions*

New claims 21-28 are non-elected because they lack the same or corresponding special technical features such as claim 1 does not require providing the buried layer after the source and drain are formed as in claim 21.

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 3, 6, and 7 are rejected under 35 U.S.C. 102(e) as being anticipated by Assaderaphi et al. (US 6,686,629).

With respect to claim 1, Assaderaphi et al. teach a semiconductor device, comprising (see fig. 1 and associated text):

a silicon body 1, in which are formed source and drain regions 11,12 defining between them a channel region 3;

a thin gate dielectric layer 4 on the channel region and a gate 5 on the thin gate dielectric layer; and

a buried layer 2 of dielectric and a thin silicon layer 3 extending between the source and drain regions and lying between the buried dielectric layer and gate dielectric layer, wherein the thin silicon layer has an area greater than that of the gate dielectric layer so that its upper surface comprises two opposed zones which extend beyond the gate dielectric layer and in that

source and drain regions each overlaps respectively, at least in part, one of said opposed zones.

With respect to claim 3, Assaderaphi et al. further teach that the buried dielectric layer extends over entire surface of the silicon body below the source and drain regions.

With respect to claim 6, Assaderaphi et al further teach that the buried dielectric layer is made of silicon dioxide or solid material. See col. 4, lines 10-15.

With respect to claim 7, Assaderaphi et al. further teach that the device is a MOS transistor.

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2, 4, 5, 11, 12, 13, 14, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Assaderaphi et al. (US 6,686,629) as applied to claims 1, 3, 6, and 7 above, and further in view of Schubert et al. (US patent 4,885,618).

With respect to claim 2, Assaderaphi et al. fail to teach that the buried dielectric layer extends between the source and drain regions.

Schubert et al. teach forming a bured dielectric region 30 between source and drain regions. See fig. 1 and associated text.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the above teaching of Schubert et al. into the device of Assaderaphi et al. to achieve shorter channel lengths to attain higher density and speed. See the abstract.

With respect to claim 4, Assaderaphi et al. further teach the device has a planar structure.

With respect to claim 5, Assaderaphi et al. teach that the buried dielectric layer is made of insulation of silicon dioxide but fail to teach the insulation is air-filled cavity.

However, the use of air-filled cavity as buried insulation is well-known.

With respect to claim 14, Assaderaphi et al. fail to teach that the gate dielectric layer is made of silicon dioxide.

However, the use of silicon dioxide as gate dielectric is well-known.

With respect to claims 11, 12, and 13, Assaderaphi et al. fail to teach the ranges for thickness of the buried dielectric layer, the ranges for the thickness of silicon channel layer, and the range for the length of the two opposed zone of silicon channel layer.

However, it would have been obvious to one of ordinary skill in the art of making semiconductor devices to determine the workable or optimal values or ranges for the thickness of the buried dielectric layer, the thickness of silicon channel layer, and the length of the two opposed zone of silicon channel layer through routine experimentation and optimization to obtain optimal or desired device performance because it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05.

With respect to claim 15, Assaderaphi et al. further teach that the source and drain regions line in the same plane as the gate.

5. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Assaderaphi et al. (US 6,686,629) in combination with Schubert et al. (US patent 4,885,618).

With respect to claim 20, Assaderaphi et al. teach a semiconductor device, comprising (see fig. 1 and associated text):

a silicon body 1, in which are formed source and drain regions 11,12 defining between them a channel region 3;

a thin gate dielectric layer 4 on the channel region and a gate 5 on the thin gate dielectric layer; and

a buried layer 2 of dielectric and a thin silicon layer 3 extending between the source and drain regions and lying between the buried dielectric layer and gate dielectric layer, wherein the thin silicon layer has an area greater than that of the gate dielectric layer so that its upper surface comprises two opposed zones which extend beyond the gate dielectric layer and in that source and drain regions each overlaps respectively, at least in part, one of said opposed zones.

Further with respect to claim 20, Assaderaphi et al. fail to teach that the buried dielectric layer extends between the source and drain regions.

Schubert et al. teach forming a bured dielectric region 30 between source and drain regions. See fig. 1 and associated text.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the above teaching of Schubert et al. into the device of Assaderaphi et al. to achieve shorter channel lengths to attain higher density and speed. See the abstract.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long Pham whose telephone number is 571-272-1714. The examiner can normally be reached on M-F, 7:30AM-3:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Long Pham
Primary Examiner
Art Unit 2814

LP